UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074

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EXAMINER
ZAMAN, FAISAL M

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/799,852	MIYANISHI ET AL.
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _05 June 2006_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _12 March 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Objections

1. Claim 19 is objected to because of the following informalities:

    In line 22-23, replace "the buffering circuit clock" to --the buffering circuit block--.

    Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1 and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by

Kasebayashi et al. ("Kasebayashi") (U.S. Patent No. 5,758,191).

Regarding Claim 1, Kasebayashi discloses a communications interface

apparatus (Figure 2, item 100, Column 4, lines 57-61) comprising:

A register circuit storing data to be transferred to a host computer (Figure 3, item

11, Column 5, lines 46-49);

A first memory storing first information indicating a specific address of the

register circuit and representing an access to the communications interface apparatus

executed by the host computer for a data transfer (Figure 3, item 12, Column 5, lines

49-52);

A second memory storing second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory (Figure 3, item 17, Column 6, lines 1-5); and

A control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed (Figure 3, item 17, Column 6, lines 5-10; although it is not specifically stated in the reference, it is understood that the data reception unit 17 comprises of both a memory and a control circuit since both functions are performed as disclosed in Kasebayashi).

Regarding Claim 10, all the same elements of Claim 1 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 10.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2, 3, 9, 11, 12, and 18** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Kasebayashi, in view of Tsuda et al. ("Tsuda") (U.S. Patent No.

6,799,242).

Kasebayashi discloses the communications interface apparatus according to

Claim 1 as described above.

Regarding Claim 2 and 3, Kasebayashi discloses wherein the control circuit

performs the information writing and reading operation for writing and reading the first

information into the first memory and the second information into the second memory in

chronological order of accesses executed (Kasebayashi, Figure 3, item 17, Column 6,

lines 5-10).

Kasebayashi does not expressly disclose wherein the control circuit performs the

information writing operation for writing the first information into the first memory and the

second information into the second memory in chronological order of accesses

executed, when an operation mode of the communications interface apparatus is

changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor (e.g. reading data from a disc for use by a

computer), Tsuda discloses wherein a control circuit performs an information writing

operation to write a first information into a first memory (Tsuda, Column 8, lines 19-21;

ie. TOC transfer command being transferred to memory control circuit 61) and a second

information into a second memory in chronological order of accesses executed (Tsuda,

Column 8, lines 21-25; ie. TOC data is transferred from SRAM 56 to buffer RAM 7),

when an operation mode of the communications interface apparatus is changed from a

low power consumption mode to a regular operation mode (Column 8, lines 11-12; ie. sleep mode to normal operational mode).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Tsuda's teachings of reading data from a disc for use by a computer to the teachings of Kasebayashi, for the purpose of providing a disc apparatus having a reduced power consumption during a sleep mode for greater efficiency in a computing system (see Tsuda, Column 3, lines 28-30). Kasebayashi also provides motivation to combine by stating it is an object of the invention to increase efficiency in a disc apparatus that communicates with a host system (see Kasebayashi, Column 2, lines 18-23).

Regarding Claim 9, the examiner takes Official Notice that the integration of a register circuit, a first and second memory, and a control circuit into a single integrated chip in the type of system disclosed was well-known in the art at the time of the Applicant's invention and the use of it would not change the scope of the invention. Therefore, it would be obvious to one of ordinary skill in the art to integrate the register circuit, the first and second memories, and the control circuit into a single integrated chip.

Regarding Claim 11, all the same elements of Claim 2 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 2 applies equally as well to Claim 11.

Regarding Claim 12, all the same elements of Claim 3 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 3 applies equally as well to Claim 12.

Regarding Claim 18, all the same elements of Claim 9 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 9 applies equally as well to Claim 18.

6. **Claims 4-6, and 13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi-Tsuda as applied to Claim 2 above, and further in view of Yamada et al. ("Yamada") (U.S. Patent No. 6,470,439).

Kasebayashi-Tsuda discloses the invention substantially as claimed.

Regarding Claim 4, Kasebayashi-Tsuda discloses wherein the control circuit conducts the information writing operations with respect to the first and second memories (Kasebayashi, Figure 3, item 12 and item 17, respectively) in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each other (Kasebayashi, Column 6, lines 1-5).

In same field of endeavor (e.g. the use of a memory control circuit in controlling memory used in various electronic devices), Yamada teaches the following limitation, which Kasebayashi-Tsuda does not expressly disclose:

Wherein a memory comprises a first-in and first-out memory (Yamada, title, abstract) including a specific number of buffer areas into which data from an external device is written (Yamada, Column 3, lines 18-31).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Yamada's teachings of the use of a memory control circuit in controlling memory used in various electronic devices with the teachings of Kasebayashi-Tsuda, for the purpose of providing a FIFO memory control circuit in which the amount of effective data in a memory can be correctly counted so that when the frequencies of a read clock and a write clock are different, data is prevented from being lost by being overwritten, and data is prevented from being read out twice (see Yamada, Column 6, lines 18-22). Kasebayashi-Tsuda provides motivation to combine by stating it is an object of the present invention to have an efficient system while reducing power consumption in a device during a sleep mode (see Tsuda, Column 3, lines 28-30).

Regarding Claim 5, Yamada discloses the following, which Kasebayashi-Tsuda does not expressly disclose:

Wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation (Yamada, Column 3, lines 26-31), and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal (Yamada, Column 4, lines 43-52).

The motivation that was utilized in the combination of Claim 4, super, applies

equally as well to Claim 5.

Regarding Claim 6, Kasebayashi-Tsuda discloses wherein the control circuit

performs the information writing and reading operation for writing and reading the first

information into the first memory and the second information into the second memory in

chronological order of accesses executed (Kasebayashi, Figure 3, item 17, Column 6,

lines 5-10) when an operation mode of the communications interface apparatus is

changed from a low power consumption mode to a regular operation mode (Tsuda,

Column 8, lines 11-12; ie. sleep mode to normal operational mode).

Kasebayashi-Tsuda does not expressly disclose wherein the information writing

and reading operation is performed without buffering the first and second information in

the first-in and first-out memories in an event that the respective first-in and first-out

memories of the first and second memories are in a memory empty state after the first

and second information stored in the respective first-in and first-out memories of the first

and second memories, respectively, are transferred to the register circuit when the

operation mode of the communications interface apparatus is changed from a low

power consumption mode to a regular operation mode.

In the same field of endeavor, Yamada teaches wherein data is not written (ie. is

not buffered) into a FIFO memory in the event that a FULL signal is sent from the

memory control circuit, indicating the FIFO memory is full (Yamada, Column 4, lines 12-

22).

The motivation that was utilized in the combination of Claim 4, super, applies equally as well to Claim 6.

Regarding Claim 13, all the same elements of Claim 4 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 4 applies equally as well to Claim 13.

Regarding Claim 14, all the same elements of Claim 5 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 5 applies equally as well to Claim 14.

Regarding Claim 15, all the same elements of Claim 6 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 6 applies equally as well to Claim 15.

7. **Claims 7-8, 16-17, and 19-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasebayashi-Tsuda-Yamada (hereinafter, "KTY") as applied to Claim 4 above in further view of Chuang et al. ("Chuang") (U.S. Patent No. 6,502,159).

KTY discloses the communications interface apparatus according to Claim 6, as described above.

Regarding Claim 7, KTY does not expressly disclose wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first

data path for the first and second information not via the first and second memories and

(ii) a second data path for the first and second information via the respective first and

second memories, on an exclusive basis according to a control signal from the control

circuit and to output corresponding data to the register circuit through the selected one

of the first and second data paths.

In the same field of endeavor (e.g. data transfers between a disk drive apparatus

and a host computer), Chuang teaches wherein a circuit (Chuang, Figure 2, item 105,

Column 4, lines 22-23) comprises a selection circuit (Chuang, Figure 3, item 120,

Column 4, lines 36-50) configured to select one of (i) a first data path for information not

via a memory (Chuang, Table 2, Column 4, lines 26-29) and (ii) a second data path for

the information via a memory (Chuang, Table 1, Column 4, lines 23-25), on an exclusive

basis according to a control signal from a control circuit (Chuang, Figure 2, item 12,

Column 3, lines 56-60) and to output corresponding data to a circuit (Chuang, Figure 3,

item 57, Column 3, lines 56-60) through the selected one of the first and second data

paths.

Accordingly, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have combined Chuang's teachings of data transfers

between a disk drive apparatus and a host computer with the teachings of KTY, for the

purpose of greatly reducing system memory usage and bus utilization (see Chuang,

Column 3, lines 52-55) and to reduce unnecessary data flow in the system and

unnecessary consumption of system resources (see Chuang, Column 3, lines 60-64).

KTY also provides motivation to combine by stating it is an object of the invention to

increase efficiency in a disc apparatus that communicates with a host system (see

Kasebayashi, Column 2, lines 18-23).

Regarding Claim 8, KTY discloses wherein the control circuit comprises:

A data writing circuit block configured to write the first and second information

into the first and second memories, respectively, in accordance with an access

performed by the host computer (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10);

A data reading circuit block configured to start reading the first and second

information from the first and second memories, respectively, upon a time the write

control circuit block starts writing the first and second information into the first and

second memories, respectively (Kasebayashi, Figure 3, item 17, Column 6, lines 5-10);

A status detecting circuit block configured to detect memory statuses of the first-

in and first-out memories included in the respective first and second memories and to

output a status signal representing the memory statuses detected (Yamada, Column 4,

lines 12-22; see combination of Claim 6 above); and

A selection control circuit block configured to control accesses to the respective

first and second memories in accordance with a status as to whether the operation

mode of the communications interface apparatus is the low power consumption mode

and the status signal output from the status detecting circuit block (Yamada, Column 4,

lines 12-22 and Tsuda, Column 8, lines 11-12; see combination of Claim 6 above).

KTY does not expressly disclose wherein the selection control circuit block is configured to control the selection circuits included in the respective first and second memories.

In the same field of endeavor, Chuang teaches wherein a selection control circuit block (Chuang, Figure 2, item 105, Column 4, lines 22-23) is configured to control the selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) included in a circuit in accordance with a status from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60).

The motivation used in the combination of Claim 7, super, applies equally as well to Claim 8.

Regarding Claim 16, all the same elements of Claim 7 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 7 applies equally as well to Claim 16.

Regarding Claim 17, all the same elements of Claim 8 are listed, but in method form rather than system form. Therefore, the supporting rationale of the rejection to Claim 8 applies equally as well to Claim 17.

Regarding Claim 19, KTY discloses an optical disk drive apparatus, comprising: an optical disk drive mechanism (Tsuda, Figure 1, Column 1, lines 19-23); and

an interface circuit for interfacing communications, between the optical disk drive

mechanism and a host computer (Kasebayashi, Figure 2, item 105, Column 4, lines 64-

66), the interfacing circuit comprising:

an input terminal for receiving data sent from the host computer (Kasebayashi,

Figure 2, see connection between items 200 and 105, Column 4, lines 64-66);

a data processor configured to perform a predetermined data processing

operation to the data received through the input terminal (Kasebayashi, Figure 2, item

101, Column 4, lines 62-64);

a clock generator configured to generate a clock signal with which the data

processor performs the predetermined data processing operation (Tsuda, Figure 7, item

62, Column 8, lines 11-25);

an operation mode changer configured to control the clock generator to reduce a

frequency of the clock signal to a value smaller than a predetermined value to change

an operation mode from a regular operation mode to a low power consumption mode

(Tsuda, Column 7 line 56 – Column 8 line 10);

a buffering circuit block configured to buffer the data received through the input

terminal (Kasebayashi, Figure 3, Column 5 line 36 – Column 6 line 13); and

a selection controller configured to control accesses to the respective first and

second memories on an exclusive basis on when the operation mode is changed from

the regular operation mode to the low power consumption mode (Yamada, Column 4,

lines 12-22 and Tsuda, Column 7, lines 57-60; see combination of Claim 6 above).

KTY does not expressly disclose wherein the buffering circuit block includes:

a first data transfer path configured to transfer the data received through the

input terminal to the data processor not via a memory, and

a second data transfer path configured to transfer the data received through the

input terminal to the data processor via a memory; and

a path selection controller configured to control the buffering circuit block to

select the second data transfer path on an exclusive basis when the operation mode is

changed from the regular operation mode to the low power consumption mode.

In the same field of endeavor, Chuang teaches wherein a circuit block includes:

a first data transfer path configured to transfer the data received through an input

terminal to a data processor (Chuang, Figure 3, item 57, Column 3, lines 56-60) not via

a memory (Chuang, Table 2, Column 4, lines 26-29), and

a second data transfer path configured to transfer the data received through the

input terminal to the data processor via a memory (Chuang, Table 1, Column 4, lines

23-25); and

a path selection controller configured to control the circuit block to select the

second data transfer path on an exclusive basis when a control circuit requests it

(Chuang, Figure 2, item 12, Column 3, lines 56-60).

The motivation used in the combination of Claim 7, super, applies equally as well

to Claim 19.

Regarding Claim 20, Chuang teaches wherein the path selection controller

selects one of the first and second data transfer paths for a write operation (Chuang,

Column 4, lines 61-64; ie. transmitting data to the system memory or to the MPEG card).

Response to Arguments

8. Applicant's arguments, see pages 11-16, filed 06/05/2006, with respect to the rejection(s) of Claims 1 and 10 under 35 USC 102(b) and Claim 19 under 35 USC 103(a) have been fully considered but they are not persuasive.

Regarding Claims 1 and 10, Applicant argues that "Kasebayashi ... does not disclose any methodology for the handling of data to be transferred to the host computer". The examiner disagrees. Contrary to Applicant's argument, Kasebayashi does in fact disclose a method of handling data to be transferred to the host computer, see Figure 3, Data Transmit Section 15 and associated Data line going from Buffer 11 to Host Computer 10, described at Column 5, lines 46-49 and lines 64-67. Applicant also argues that Tsuda (see page 14) and Chuang (see page 15) do not disclose the limitations of claims 1 and 10, however the examiner notes that neither of these references were used in the rejection of Claims 1 and 10 in the Office Action dated 03/06/2006.

Regarding Claim 19, in response to applicant's arguments against the references individually (see generally pages 13-16), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Therefore, the rejections to Claims 1, 10, and 19 stand as previously rejected.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

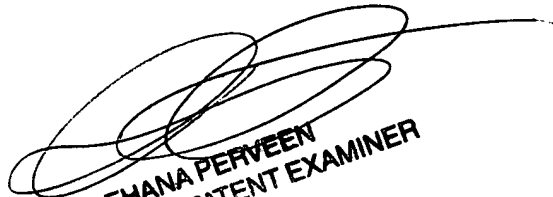than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Faisal Zaman whose telephone number is 571-272-

6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm

(every-other-Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the
Patent Application Information Retrieval (PAIR) system. Status information for
published applications may be obtained from either Private PAIR or Public PAIR.
Status information for unpublished applications is available through Private PAIR only.
For more information about the PAIR system, see http://pair-direct.uspto.gov. Should
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fmz

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7/3/06